

Wafer-sort bring-up: top ten corrective actions and lessons learned

1 Corrective actions, ranked by leverage on the sort-flow validation date

#	Bone	Corrective action	Owner	By
1	Tester access	Pin the foundry tester consignment date; if none within a week, commit to the prober rental and the tester days already offered	COO / site director	Week 1
2	Probe card	Pull in the production card; in parallel, run pins-up compile and runtime debug on the engineering card so code is ready when the card lands	Test consultant / lead test engineer	Week 1
3	Test code	Put all sort and final-test code in a shared repository; no further rewrites from scratch, branch and merge only	Offshore test lead	Week 1
4	Documentation	Name one owner for the remaining sort and final-test specs; close the open clarifications and freeze a strict-sequence rewrite	Design engineering	Week 2
5	Serial work	Split the test team so sort 2 and the laser fusing program run in parallel with the sort 1 redundancy tests; link fusing after sort 1, not sort 2	Offshore test lead / PM	Week 1
6	Skills	Convert the one-month redundancy contractor to three months and put a second engineer inside the binning logic with the lead designer	COO	Week 2
7	Communication	Standing weekly design-to-test working session with both sites on the same call; test team embedded at the foundry from card arrival through first wafer	PM	Weekly
8	Governance	Flag the probe card, foundry tester and sort-program chain as critical in the plan so the weekly refresh shows the negative float	PM / scheduler	Next refresh
9	Decisions	Decide first-silicon-without-repair, wafer dicing for two prober stations, and the burn-in venue at the next taskforce; no decision carries past week 2	Lead designer / process lead	Week 2
10	People load	Scrub the four people carrying 44 to 92 open tasks each; move pattern generation and bench automation to idle digital designers	COO / PM	Week 2

2 Lessons learned for the next development project

Lesson for the next development project	What it cost on this program
Order long-lead test hardware at tapeout, not at first silicon	Card ordered at first silicon, criticality recognized two months later, delivered four months after that; silicon waited
Put a test engineer in the room for every DFT decision	No BIST, manual trim and a first-silicon timing issue were all absorbed by test as workarounds
Hand over test with a finished, strict-sequence spec and a shared code repository	Five weekly cycles to transfer ownership; three months with no coding; code regenerated from scratch
Co-locate for first-silicon bring-up; web meetings do not carry a complex spec	The test lead asked to send engineers to the design site; approved only after routing through a third party
Contract tester access before the plan commits to it	Consignment at 57% with no date; rental impossible the month it was needed; the chain slipped 30 days in four baselines
Limit single-person ownership on the critical chain	Four people each carry 44 to 92 open tasks; one departure reshuffles three workstreams
Recompute float every refresh and flag the real critical chain	The sort chain ran at -57 to -60 d to the MVP target without appearing on the plan's critical path
Decide binning cut-lines, burn-in and data path with product and quality owners, not test	Still unowned after five months; test absorbs revenue decisions by default

Sources: the cause-and-effect analysis, the project schedule, weekly refresh minutes and executive correspondence. Client, people, vendors and calendar dates generalized; owners are roles and weeks count from the escalation meeting.