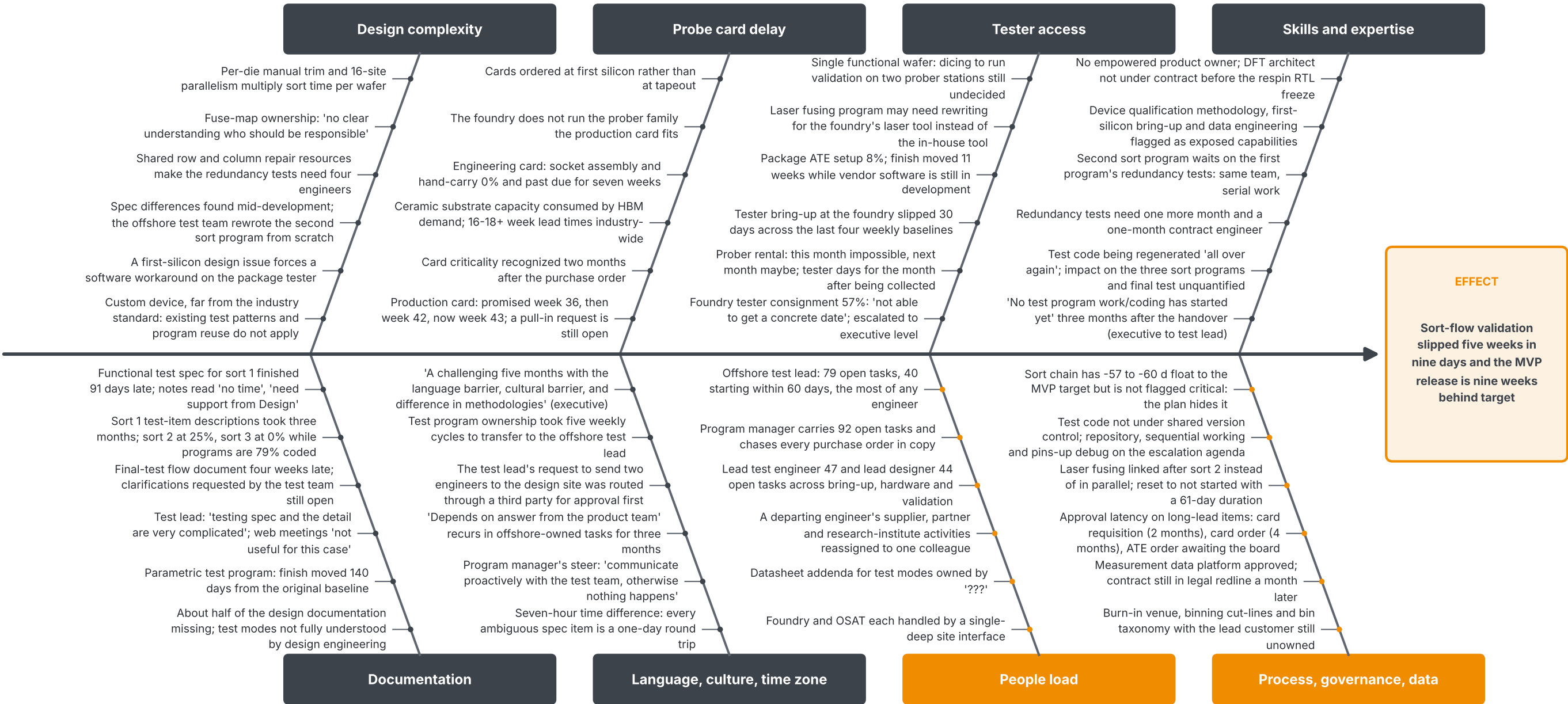


Why wafer-sort bring-up is late and slow: cause-and-effect analysis



What the schedule says (finish dates, original baseline vs current plan, in program weeks; target where one exists)

Production probe cards developed and tested wk 40 → wk 46	+44 d	Tester bring-up at the foundry sorted wk 43 → wk 47	+30 d	Sort 1 functional test program completed wk 42 → wk 48	+41 d	Sort test program completed wk 40 → wk 49	+59 d	Full sort flow validated wk 44 → wk 49	+32 d	Package tester ready wk 41 → wk 52	+76 d	Respin 0: MVP released to lead customer wk 70 tgt → wk 79	-67 d
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■ Problem areas named by the client's executive ■ Added from the program record; quotes are verbatim from minutes and correspondence

Sources: Project schedule (tasks, notes, eleven saved baselines, independent CPM recompute); weekly refresh minutes; executive correspondence; test-readiness and risk memos. Client, people, vendors and calendar dates generalized.