

**Goal: select optimal schedule acceleration approach for Sumatra**

- helps to win customer(s) through early proof of concept (L: .441)
- speeds up schedule (L: .404)
- minimizes marketing risk (L: .081)
- lowest R&D cost (L: .074)

1. NFC PHY only + super hot lot	.138
2. super hot lot + soft macro + outsource resources	.110
3. bread-board demo + outsource resources	.260
4. NFC PHY only + bread-board demo + outsource resources	.491

Expert Choice C:\Documents and Settings\Neal Mitchell\Desktop\sum...

File Edit

Distributive mode  Ideal mode

Summary | Details

Sort by Name  Unsort

Synthesis with respect to: Goal: select optimal schedule acceleration approach for Sumatra

Overall Inconsistency = .10

4. NFC PHY only + bread-board demo + outsource resources	.491	<div style="width: 100%;"></div>
3. bread-board demo + outsource resources	.260	<div style="width: 53%;"></div>
1. NFC PHY only + super hot lot	.138	<div style="width: 28%;"></div>
2. super hot lot + soft macro + outsource resources	.110	<div style="width: 22%;"></div>

## Information Document

**Milestone: 1st Engineering Samples Delivered****Cost of Delay = ~\$75k/day lost PBT****Top 5 Current Thinking Elements to Challenge & Their Alternatives:**

- Combined BT & NFC  
-->alternative: **NFC PHY Only** (saves 7 weeks)
- Not super hot lot  
-->alternative: **do super hot lot** (saves 2 weeks)
- Using ARM7 hard macro  
-->alternative: **use soft-macro** (saves 2 weeks)
- Limited resources (prevents further slip caused by resources being lost to Bali)  
-->alternative: **outsource digital design**/get ex-S.J. team
- Si samples on reference design (saves 20 weeks)  
-->alternative: **bread-board demo** (FPGA+discrete radio PHY, digital)

**Brainstormed Current Thinking:****Dominating Ideas**

- provide early demo to customers of minimal functionality
- Si samples (not FPGA) on reference design delivered on evaluation platform
- combined NFC+BT solution (vs. stand alone NFC)

**Assumptions**

- 1st Sample is functional (supports 1-mode of NFC operation)
- interface assumptions (still not ratified by standards board) --guess on ESD interface
- leverage Bali, assumes Bali P&R is clean
- funding is available
- not a super hot lot

**Essential Factors**

- IP development from IRT
- 106 kbps operation in positive mode

**Boundry Conditions**

- limited resources
- UMC 0.1 micron
- senior management approval of IP (ARM soft-macro)
- can't hire new headcount

**Avoidance**

none listed